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EXAMINER	
HAILE, FEBEN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/021,439	CHOI, SANG JUN	
	Examiner	Art Unit	
	Feben M. Haile	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-4,7-12,14 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-4,7-12,14 and 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In view of applicant's amendment filed November 23, 2007, the status of the application is still pending with respect to claims 1, 3-4, 7-12, 14, and 16-26.

2. The amendment filed is insufficient to overcome the rejection of claims 1-4, 7-12, 14, and 16-26 based upon Dempo (US 6,594,267) as set forth in the last Office action because: the material added to the claims fail to further clarify a distinction between the Applicants invention and the cited reference, thus the subject matter is not patentable.

3. The Examiner acknowledges the cancellation of claim 6, thus it has been withdrawn from consideration.

Claim Rejections - 35 USC § 102

The following is a quotation of 35 U.S.C. 102(b) which forms the basis for all obviousness rejections set forth in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-4, 6-12, 14, and 16-26 rejected under 35 U.S.C. 102(b) as being unpatentable over Dempo (US 6,594,267), hereinafter referred to as Dempo.

Regarding claim 1, Dempo discloses a) dividing an input ATM adaptation layer 2 (AAL2) cell into AAL2 type common part sublayer (CPS) packets **(figure 4; column 8**

lines 4-5; a selector 11 extracts CPS-PDUs from ATM cells); b) sequentially storing the divided CPS packets into first storage areas, with each first storage area corresponding to a different one of a plurality of virtual paths/virtual channels (VPs/VCs) of the respective CPS packets, and sequentially storing first identifiers of the first storage areas, each first identifier corresponding to a different one of the first storage area **(figure 4; column 8 lines 5-10; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and figures 4-5; column 8 lines 4-10; addresses #1 concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address #1 corresponds to different VPI & VCI)**; c) reading the stored first identifiers, sequentially storing the read CPS packets in second storage areas used to route the CPS packets to each destination, wherein each second storage area corresponds to a different one of a plurality of channel identifiers (CIDs), and sequentially storing second identifiers of the second storage areas, each second identifier corresponding to a different one of the second storage areas and to a different one of the plurality of CIDs, wherein the sequential storing the second identifiers includes generating a second reference table that maps each of the second identifiers to corresponding one of the plurality of destination CIDS **(figure 4; column 8 lines 11-13 & 23-31; a processing section 17 extracts CPS packets from the CPS-PDUs stored in the FIFO memory 12 and a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address concerning each of the CPS packets are stored in FIFO memory 19; figures 4-5; column 8 lines 23-31; a FIFO memory 18 stores CPS**

packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19, where each address #2 corresponds to an output CID; column 20 lines 5-27; the processing section 17 executes a CID alteration method to prevent CID collision between CPS packets; figure 5; column 18 lines 55-58; a path setting table maps addresses #2 with output CIDs); and d) reading the CPS packets, in the order of the second identifiers, from the second storage areas and multiplexing the read CPS packets to generate a reconstructed AAL2 cell **(figure 4; column 31-40; the CPS packets stored in FIFO memory 18 which have the same address are multiplexed to generate a CPS-PDU to which an ATM cell header is added thus creating an ATM cell;)**, wherein c) comprises changing origination CIDs of the read CPS packets to corresponding destination CIDs, and sequentially storing the read CPS packets in the second storage areas corresponding to the destination CIDs **(figures 4-5; column 20 lines 5-27; the processing section 17 alters input CID information to output CID information and figures 4-5; column 8 lines 23-31; the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address #2 concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an input and output CID)**.

The claimed step of ***sequentially storing*** reads on ***a FIFO memory*** since this principle is based on a first come, first serve behavior. It is analogous to the behavior of persons standing in line, where the persons leave in the order they arrive. Therefore

as the claims are interpreted in their broadest sense, the Examiner believes that this standard is equivalent to the step of sequentially storing.

Regarding claim 3, Dempo discloses wherein the CPS packets are stored in the first and second storage areas according to their respective order of arrival **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and the FIFO memory 18 stores CPS packets outputted by the processing section 17)**.

Regarding claim 4, Dempo discloses wherein the CPS packets are read from the first and second storage areas according to their respective order of storage **(one of ordinary skill in the art recognizes the well known practice of transmitting packets from storage units by the order of their arrival)**.

Regarding claim 7, Dempo discloses wherein the first and second identifiers are stored in the order that the CPS packets ate stored to the corresponding first and second storage areas, respectively **(figures 4-5; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in the FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address has corresponding VPI, VCI, & CID information and a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19; where each address has corresponding VPI, VCI, & CID information)**.

Regarding claim 8, Dempo discloses wherein the CPS packets are read from the first and second storage areas according to their respective order of storage **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and the FIFO memory 18 stores CPS packets outputted by the processing section 17)**.

Regarding claim 9, Dempo discloses implementing a switching test by reading the CPS packets from the second storage areas **(figure 4; column 11 lines 6-23; a CPS-PDU processing section reads out a CPS packet from a memory according to its corresponding address and also executes a parity check)**.

The claimed step of ***in the order of the second identifiers*** reads on ***in the order of their arrival*** since this principle is based on the practice of positioning packets in storage units by the order of their arrival and transmitting the packets from the storage units by the order of their arrival. Therefore as the claims are interpreted in their broadest sense, the Examiner believes the order of their arrival is equivalent to the order of the second identifiers.

Furthermore, the claimed step of ***comparing the read CPS packets to a standard*** reads on ***according to a parity check*** since this principle is based error detection, which can be performed using header error control, which is an IEEE 802.11b standard. Therefore as the claims are interpreted in their broadest sense, the Examiner believes a parity check is equivalent to the step of comparing the read CPS packets to a standard.

Regarding claim 10, Dempo discloses implementing a switch signaling by reading the CPS packets from the second storage areas and outputting the read CPS packets to a processor **(figure 4; column 8 lines 5-10 & 23-31; the FIFO memory 18 stores CPS packets outputted by the processing section 17)**.

The claimed step of ***in the order of the second identifiers*** reads on ***in the order of their arrival*** since this principle is based on the practice of positioning packets in storage units by the order of their arrival and transmitting the packets from the storage units by the order of their arrival. Therefore as the claims are interpreted in their broadest sense, the Examiner believes the order of their arrival is equivalent to the order of the second identifiers.

Regarding claim 11, Dempo discloses routing the CPS packets stored in the first storage areas to another switch **(figure 4; column 8 lines 5-10; the CPS-PDUs are stored in a FIFO memory 12)**.

The claimed step of ***in the order of the first identifiers*** reads on ***in the order of their arrival*** since this principle is based on the practice of positioning packets in storage units by the order of their arrival and transmitting packets from the storage units by the order of their arrival. Therefore as the claims are interpreted in their broadest sense, the Examiner believes the order of their arrival is equivalent to the step of comparing to the order of the first identifiers.

Regarding claim 12, Dempo discloses wherein the first and second storage areas have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of**

the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19).

Regarding claim 14, Dempo discloses a reassembly processing unit that divides an input-ATM adaptation layer (AAL2) cell into AAL2 type common part sublayer (CPS) packets **(figure 4; column 8 lines 4-5; a selector 11 extracts CPS-PDUs from ATM cells)**; a first memory that sequentially stores the divided CPS packets into first storage areas with each first storage area corresponding to a different one of a plurality of virtual paths/virtual channels (VPs/VCs) and that sequentially stores first identifiers of the first storage areas, each first identifier corresponding to a different one of the first storage areas and to a different one of the plurality of VPs/VCs, wherein the first memory includes a first reference table that maps the first identifiers to the corresponding one of the plurality of VPs/VCs **(figure 4; column 8 lines 5-10; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13; figures 4-5; column 8 lines 4-10; addresses #1 concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address #1 corresponds to different VPI & VCI; figure 5; column 18 lines 55-58; a path setting table maps addresses #1 with input VPIs and VPCs)**; a CPS packet switching unit that reads the stored CPS packets from the first storage areas in the order of the stored first identifiers and routes the read CPS packets to each destination **(figure 4; column 8 lines 11-13; a processing section 17 extracts CPS packets from the CPS-PDUs stored in the FIFO memory 12)**, a second memory that

sequentially stores the routed CPS packets into second storage areas with each second storage area corresponds to a different one of a plurality of destination channel identifiers (CIDs), and sequentially stores second identifiers of the second storage areas, each second identifier corresponding to a different one of the second storage areas and to a different one of the plurality of destination CIDs, wherein the second memory includes a second reference table that maps the second identifiers tot he corresponding one of the plurality of destination CIDs **(figure 4; column 8 lines 23-31; a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19; column 20 lines 5-27; the processing section 17 executes a CID alteration method to prevent CID collision between CPS packets; figure 5; column 18 lines 55-58; a path setting table maps addresses #2 with output CIDs)**; and an assembly processing unit that reads the CPS packets from the second storage areas in the order of the second identifiers and multiplexes the CPS packets read from the second storage areas to generate a reconstructed AAL2 cell **(figure 4; column 31-40; the CPS packets stored in FIFO memory 18 which have the same address are multiplexed to generate a CPS-PDU to which an ATM cell header is added thus creating an ATM cell)**, wherein the CPS packet switching unit changes origination channel identifiers (CIDs) of the CPS packets read from the first storage areas to corresponding destination CIDs and sequentially stores the read CPS packets in the second storage areas corresponding to the destination CIDs **(figures 4-5; column 20 lines 5-27 & column 8 lines 23-31; the processing section 17 alters input CID**

information to output CID information and the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an input and output CID).

The claimed step of sequentially storing reads on a FIFO memory since this principle is based on a first come, first serve behavior. It is analogous to the behavior of persons standing in line, where the persons leave in the order they arrive. Therefore as the claims are interpreted in their broadest sense, the Examiner believes that this standard is equivalent to the step of sequentially storing.

Regarding claim 16, Dempo discloses first, second, third, and fourth memories that sequentially store ATM adaptation layer 2 (AAL2) type common part sublayer (CPS) packets and output the CPS packets in order of their respective storage, wherein each memory has a plurality of storage areas **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19)**; a reassembly processing unit that divides an input AAL2 cell into the AAL2 type CPS packets, stores the divided CPS packets in different first storage areas of the first memory with each first storage area corresponding to a different one of a plurality of virtual paths/virtual channels (VPs/VCs), and stores first identifiers of the different first storage areas in the second memory, each first storage area having a different first identifier that corresponds to one of the plurality of VPs/VCs

(figures 4-5; column 8 lines 4-10; a selector 11 extracts CPS-PDUs from ATM cells and the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses #1 concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address corresponds to a different VPI & VCI); a CPS packet switching unit that reads the CPS packets stored in the first memory in an order of the first identifiers stored in the second memory, stores the read CPS packets in different second storage areas of the third memory with each second storage area corresponding to a different one of a plurality of destination channel identifiers (CIDs), and stores second identifiers of the second storage areas in the fourth memory, each second storage area having a different second identifier that corresponds to one of the plurality of destination CIDs **(figures 4-5; column 8 lines 23-31; a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an output CID; column 20 lines 5-27; the processing section 17 executes a CID alteration method to prevent CID collision between CPS packets)**; and an assembly processing unit that reads the CPS packets stored in the third memory in the order of the second identifiers stored in the fourth memory and multiplexes the read CPS packets to generate a reconstructed AAL2 cell **(figure 4; column 31-40; the CPS packets stored in FIFO memory 18 which have the same address are multiplexed to generate a CPS-PDU to which an ATM cell header is added thus creating an ATM cell)**.

The claimed step of sequentially storing reads on a FIFO memory since this principle is based on a first come, first serve behavior. It is analogous to the behavior of persons standing in line, where the persons leave in the order they arrive. Therefore as the claims are interpreted in their broadest sense, the Examiner believes that this standard is equivalent to the step of sequentially storing.

Regarding claim 17, Dempo discloses a first reference table that maps the first identifiers with the corresponding VPs/VCs **(figure 5; column 18 lines 55-58; path setting table maps addresses #1 with input VPIs and VCIs)**; and a second reference table that maps the second identifiers with the corresponding destination CIDs **(figure 5; column 18 lines 55-58; path setting table maps addresses #2 with output CIDs)**.

Regarding claim 18, Dempo discloses wherein the reassembly processing unit refers to the first reference table to determine the first storage areas corresponding to the VPS/VCS of the CIDS packets **(figures 4-5; column 8 lines 5-10; the selector 11 receives the addresses concerning the CPS-PDUs and stores them FIFO memory 13, where each address corresponds to a VPI & VCI)**.

Regarding claim 19, Dempo discloses wherein the CPS packet switching unit refers to the second reference table to determine the respective destination CIDs corresponding to the CPS packets **(figures 4-5; column 8 lines 23-31; the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to a output CID)**.

Regarding claim 20, Dempo discloses wherein the CPS packet switching unit changes origination CIDs of the CPS packets read from the fist memory to the corresponding destination CIDs, with reference to the second reference table **(figures 4-5; column 20 lines 5-27 & column 8 lines 23-31; the processing section 17 alters input CID information to output CID information and the FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile address concerning each of the CPS packets are stored in FIFO memory 19, where each address corresponds to an input and output CID)**.

Regarding claim 21, Dempo discloses wherein the first and second identifiers are stored in the order that the CPS packets are stored to the corresponding first and second storage areas, respectively **(figures 4-5; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13, where each address has corresponding VPI, VCI, & CID information and a FIFO memory 18 stores CPS packets outputted by the processing section 17, meanwhile addresses #2 concerning each of the CPS packets are stored in FIFO memory 19; where each address has corresponding VPI, VCI, & CID information)**.

Regarding claim 22, Dempo discloses wherein the first, second, third, and fourth memories have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18**

stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19).

Regarding claim 23, Dempo discloses a central processing unit that reads the CIDS packets from the first memory in the order of the stored first identifiers and implements testing and signaling for switching **(figure 4; column 11 lines 6-23; a CPS-PDU processing section reads out a CPS packet from a memory according to its corresponding address and also executes a parity check)**.

Regarding claim 24, Dempo discloses wherein the first, second, third, and fourth memories have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19)**.

Regarding claim 25, Dempo discloses a plurality of cell switches that each has first, second, third, and fourth memories **(figure 4; FIFO memories 12-13 and 18-19)**, a reassembly processing unit **(figure 4; selector 11)**, a CPS packet switching unit, and an assembly processing unit **(figure 4; packet processing section 17)**; and a router that routes the CPS packets output from one of the plurality of cell switches to another cell switch **(figure 4; multiplexing section 27)**.

Regarding claim 26, Dempo discloses wherein the first, second, third, and fourth memories have a queue type structure **(figure 4; column 8 lines 5-10 & 23-31; the CPS-PDUs are stored in a FIFO memory 12, meanwhile addresses concerning**

each of the CPS-PDUs are stored in FIFO memory 13 and a FIFO memory 18 stores CPS packets, meanwhile addresses concerning each of the CPS packets are stored in FIFO memory 19).

Response to Arguments

5. Applicant's arguments filed November 23, 2007 have been fully considered but they are not persuasive.

The Applicant respectfully traverses that Dempo fails to teach or suggest each first storage area corresponding to a different one of a plurality of VPs/VCs, wherein each first identifiers corresponds to a different one of the first storage areas and to a different one of the plurality of Virtual Paths/Virtual Channels. The Examiner respectfully disagrees. Dempo discloses storing CPS-PDUs in one FIFO memory meanwhile addresses concerning each of the CPS-PDUs are stored in another FIFO memory. Dempo goes on to suggest a path setting table including the addresses concerned with each of the CPS-PDUs and corresponding different ones of Virtual Path/Channel Identifiers.

The Applicant respectfully traverses that Dempo fails to teach or suggest storing the read CPS packets in second storage areas used to route the CPS packets to each destination, wherein each second storage area corresponds to a different one of a plurality of destination channel identifiers. The Examiner respectfully disagrees. Dempo discloses storing CPS packets outputted from a processing section in one FIFO memory meanwhile addresses concerning each of the CPS packets are stored in

another FIFO memory. Dempo further suggests a path setting table including the addresses concerned with each of the CPS packets and corresponding Channel Identifiers, whereby the processing section 17 executes a CID alteration method to prevent CID collision between CPS packets.

The Applicant respectfully traverses that Dempo fails to disclose that the step of storing is being done sequentially. The Examiner respectfully disagrees. The method of storing information in the memory using a FIFO operation is based on a first come, first serve behavior using read and write pointers, where information is processed in the order they arrive. It is analogous to the behavior of persons standing in line, where each person (packets) with an associated write pointer (identifier) takes up a particular spot in the line (storage areas) and leaves the line in the order they arrived (sequentially).

Therefore, as the claims are interpreted in their broadest sense, the Examiner believes that Dempo indeed does render the Applicant's invention obvious.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Feben M. Haile whose telephone number is (571) 272-3072. The examiner can normally be reached on 6:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571) 272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

02/01/2008

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